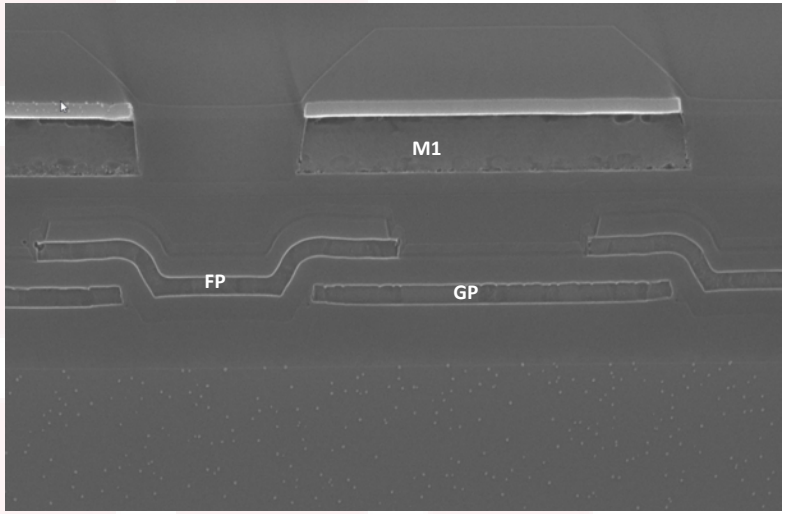
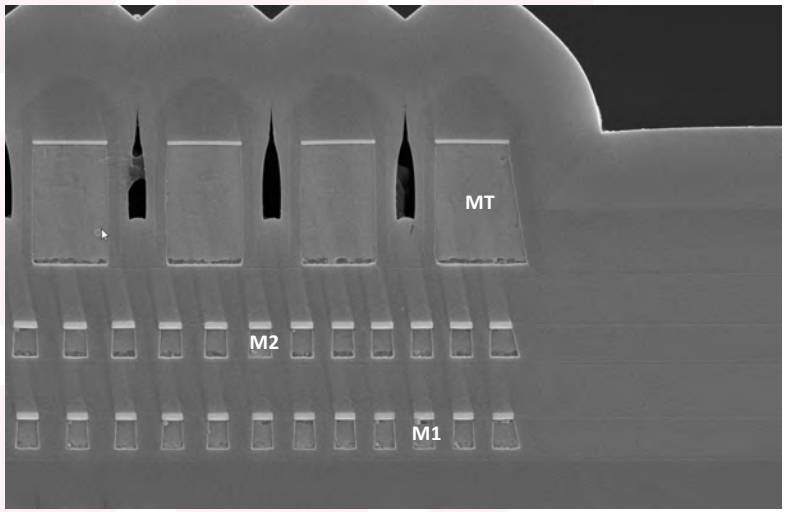
1200V BCD Technology

- **SG7UHV is a 24 (+1 optional) layer high voltage (1200V) BCD technology with dual gate and 3LM.**

Item	SG7UHV
Design rules	0.50um (FEOL), 0.30um (BEOL)
Process	3BL-EPI 2P/3M
Mask count	24L + 1L op
Epi	7.0um, 4.57ohm-cm
GOX	180A / 800A
CMOS	NMOS: 0.8um PMOS: 0.6um
Isolation	LOCOS/JI
Silicidation	CoSi
M1/M2 (Tk)	0.5um
MT (Tk)	2.0um
CMOS	5V/7V/20V/30V
Bipolar	7V/20V/40V
Diode	6V
Capacitor	PI-Poly, Poly-Top metal
Resistor	2.5Kohm/sq
LDMOS	1200V





Layer name.	Layer description
LN	N-type lightly doped buried well
NB	N-type buried layer
PB	P-type buried layer
DE	Device, Active
PW	HV Pwell
PL	N Plug (Optional)
PI	P-isolation diffusion
LVPW	LV Pwell
LVNW	LV Nwell
RP	N+ Poly doping
GP	Gate polysilicon
NLD	N-MOS LDD
PLD	P-MOS LDD
NP	N+ S/D
PP	P+ S/D
FP	Field polysilicon
SB	Salicide Block
CT	Contact
M1	Metal1
V1	Via1
M2	Metal2
V2	Via2
MT	Top metal
PA	Passivation open
BC	Buffer coat