40V MOSFET Technology detail

- "Split-gate Transistor/ SGT" Discrete MOSFET (two different isolated poly in trench)
- 7 masking layers (including Passivation)
  - TR (trench)
  - FP (field plate poly)
  - G (active)
  - BS (source implant)
  - CT (contact)
  - AL (top metal)
  - PIF (passivation)
- 40V max source-drain rating, state of the art RSP
- 500A Gate oxide thickness, VTH = 3.0 V
- 1.3 um unit cell pitch, 2.6 um trench depth
- Vertical recess metrology + APC for control of vertical dimensions
- Dual layer epi, oxide CMP and poly CMP